

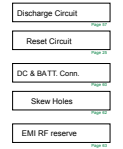
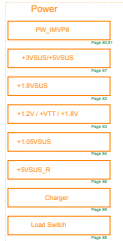
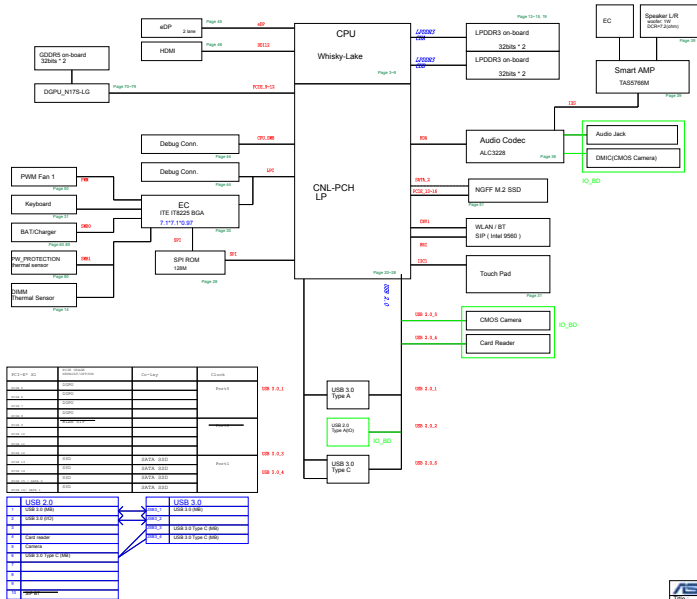


SYSTEM PAGE REF.

PAGE	Content
1	Block Diagram
2	System Setting
3	CPU_DISPLAY
4	CPU_DISPLAY
5	CPU_LPC,SP7,SMB,CLINK
6	CPU_POWER
7	CPU_KDP
8	CPU_MISC,VTAG,CLK
9	CPU_CFG,SVID
10	CPU_POWER_CAP
11	TST_Alpha-Ridge
12	TSTATSP65552type_C_port1
13	LPDDR3_THERMISTATION
14	LPDDR3_ON-BOARD_A
15	LPDDR3_ON-BOARD_B
16	
17	LPDDR3_CA_OG_VOLTAGE
18	CPU_PCH_CPU_DISPLAY
19	CPU_PCH_CFG_DISPLAY
20	CPU_PCH_CFG_DISPLAY
21	CPU_PCH_CFG_DISPLAY
22	CPU_PCH_CFG_DISPLAY
23	CPU_PCH_CFG_DISPLAY
24	CPU_PCH_CFG_DISPLAY
25	CPU_PCH_CFG_DISPLAY
26	CPU_PCH_CFG_DISPLAY
27	CPU_PCH_CFG_DISPLAY
28	CPU_PCH_CFG_DISPLAY
29	CPU_PCH_CFG_DISPLAY
30	CPU_PCH_CFG_DISPLAY
31	CPU_PCH_CFG_DISPLAY
32	CPU_PCH_CFG_DISPLAY
33	CPU_PCH_CFG_DISPLAY
34	CPU_PCH_CFG_DISPLAY
35	CPU_PCH_CFG_DISPLAY
36	CPU_PCH_CFG_DISPLAY
37	CPU_PCH_CFG_DISPLAY
38	CPU_PCH_CFG_DISPLAY
39	CPU_PCH_CFG_DISPLAY
40	CPU_PCH_CFG_DISPLAY
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71	CPU_PCH_CFG_DISPLAY
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73	CPU_PCH_CFG_DISPLAY
74	CPU_PCH_CFG_DISPLAY
75	CPU_PCH_CFG_DISPLAY
76	CPU_PCH_CFG_DISPLAY
77	CPU_PCH_CFG_DISPLAY

## UX433 SCHEMATIC Revision 0.1

## BLOCK DIAGRAM

FA: UMA  
FR: DGPU=Nvidia MX150 + V2G

[illegible][illegible][illegible]

BIO 100L ANDIG 100L		
Lab Section		
100-Bio 100L1	100-Bio 100L10	
100-Bio 100L2	100-Bio 100L11	
100-Bio 100L3		
100BIO 100L 100L 100L	100L	
100-Bio 100L4	100L	
100-Bio 100L5	100L	
100-Bio 100L6	100L	
100-Bio 100L7	100L	
100-Bio 100L8	100L	
100-Bio 100L9	100L	
100-Bio 100L10	100L	
100-Bio 100L11	100L	
100-Bio 100L12	100L	
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100-Bio 100L37	100L	
100-Bio 100L38	100L	
100-Bio 100L39	100L	
100-Bio 100L40	100L	
100-Bio 100L41	100L	
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100-Bio 100L44	100L	
100-Bio 100L45	100L	
100-Bio 100L46	100L	
100-Bio 100L47	100L	
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100-Bio 100L49	100L	
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100-Bio 100L80	100L	
100-Bio 100L81	100L	
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100-Bio 100L87	100L	
100-Bio 100L88	100L	
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100-Bio 100L91	100L	
100-Bio 100L92	100L	
100-Bio 100L93	100L	
100-Bio 100L94	100L	
100-Bio 100L95	100L	
1		

PS001-2	100%	PS001-3	100%
PS001-4	100%	PS001-5	100%
PS001-6	100%	PS001-7	100%
PS001-8	100%	PS001-9	100%
PS001-10	100%	PS001-11	100%
PS001-12	100%	PS001-13	100%
PS001-14	100%	PS001-15	100%
PS001-16	100%	PS001-17	100%
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PS001-50	100%	PS001-51	100%
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PS001-54	100%	PS001-55	100%
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PS001-58	100%	PS001-59	100%
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PS001-64	100%	PS001-65	100%
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PS001-86	100%	PS001-87	100%
PS001-88	100%	PS001-89	100%
PS001-90	100%	PS001-91	100%
PS001-92	100%	PS001-93	100%
PS001-94	100%	PS001-95	100%
PS001-96	100%	PS001-97	100%
PS001-98	100%	PS001-99	100%
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PS001-102	100%	PS001-103	100%
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PS001-122	100%	PS001-123	100%
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PS001-148	100%	PS001-149	100%
PS001-150	100%	PS001-151	100%
PS001-152	100%	PS001-153	100%
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PS001-156	100%	PS001-157	100%
PS001-158	100%	PS001-159	100%
PS			

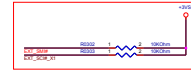
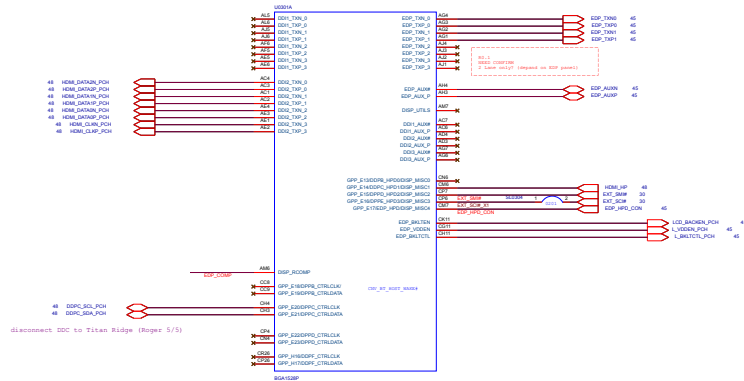
Primary Insurance Carrier		
IC#		
State		
Secondary Insurance Carrier		
IC#	0000000000	0000000000
State		



EDP	EDP
DDI1	N/A
DDI2	HDMI

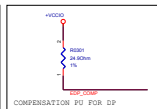
Intel Version	ASUS P/N
ES-0	01001-01540000
ES-1	01001-01640000
ES-2	01001-01660100
	01001-01660000

81.0  
0427  
Follow FPM Request Line V04



PDG#543016 DDI1 mapping DDPM  
DDI2 mapping DDPC

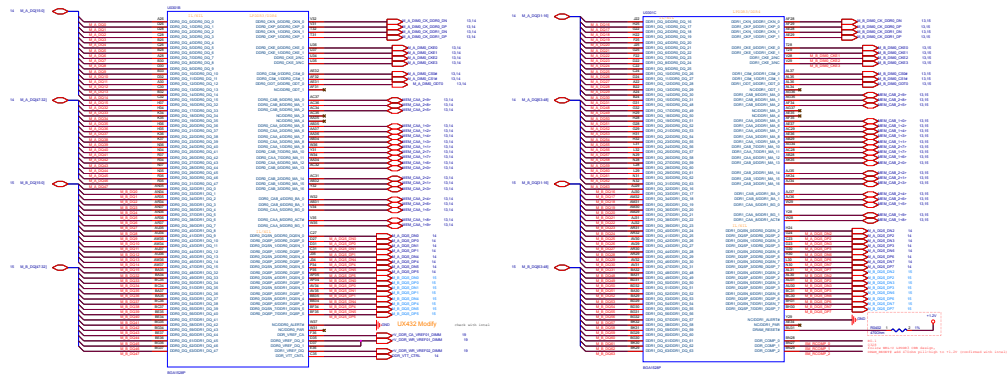
	HDMI
DDI2_0	Lane2
DDI2_1	Lane1
DDI2_2	Lane0
DDI2_3	CLK
DDPC	I2C



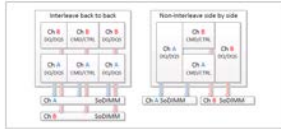
Page. 147

		Project Name		Rev
UX432				R1
Title : CPU_DSPBA				
Size Custom	Dept.: ASUS/TK COMPUTER INC.		Engineer: Tony1_chang	
Date: Wednesday, July 18, 2018		Sheet	3	of 100

LPDDR3 Non-Interleaved

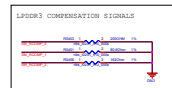


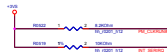
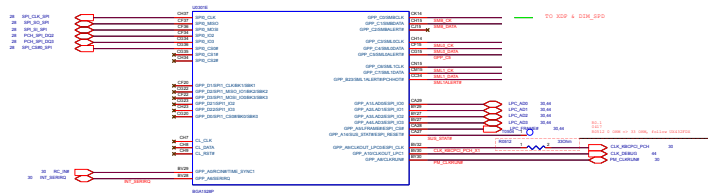
IL		NIL	
Channel	Byte	Channel	Byte
D0R0	Byte0	D0R0	Byte0
D0R0	Byte1	D0R0	Byte1
D0R0	Byte2	D0R0	Byte2
D0R0	Byte3	D0R0	Byte3
D0R0	Byte4	D0R1	Byte0
D0R0	Byte5	D0R1	Byte1
D0R0	Byte6	D0R1	Byte2
D0R0	Byte7	D0R1	Byte3
D0R1	Byte0	D0R1	Byte4
D0R1	Byte1	D0R1	Byte5
D0R1	Byte2	D0R1	Byte6
D0R1	Byte3	D0R1	Byte7
D0R1	Byte4	D0R1	Byte0
D0R1	Byte5	D0R1	Byte1
D0R1	Byte6	D0R1	Byte2



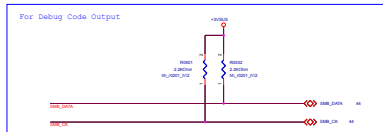
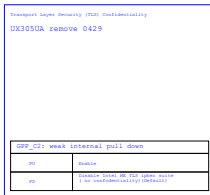
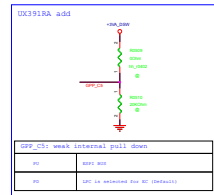
Platform	Config #	Tech	Topology	Max Freq	Memory Device	Device Rb/Wt	Pack Stck-up	IU/MLT/VTL
CFL-U LPDDR3	Chapter 4.2.1	LPDDR3	1R x32	1860/2133	QOP (1 x 32 db)		Nil	
			2R x32	1860/2133	QOP (2 x 32 db)	178	(1 x 34)	Nil
			2R x32	1860/2133	QOP (4 x 16 db)			
	Chapter 4.2.2	LPDDR3	1R x64	1860/2133	QOP (2 x 32 db)		Nil	
			2R x64	1860/2133	QOP (4 x 32 db)	251	(3 x 34)	Nil

Project Name	Region	Funding Source	Plan Length (km)		Project Start Date	Project End Date	Project Status	Project Manager	Project Description	Project Budget (€)	Project Impact
			Plan Length (km)	Plan Length (km)							
Project A	North	Government	100	100	2010	2015	Completed	John Doe	Infrastructure development	1000000	High
Project B	South	Private	150	150	2012	2017	In Progress	Jane Smith	Infrastructure development	1500000	Medium
Project C	West	Government	200	200	2015	2020	Planned	John Doe	Infrastructure development	2000000	High
Project D	East	Private	250	250	2018	2023	Planned	Jane Smith	Infrastructure development	2500000	Medium





UX305UA CRB 1.1 P.20 150K PU ok 0318 change to 100K 0324



TP for Boundary Scan Test

02.1  
0409  
Remove TC603 for layout purposes.

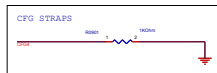
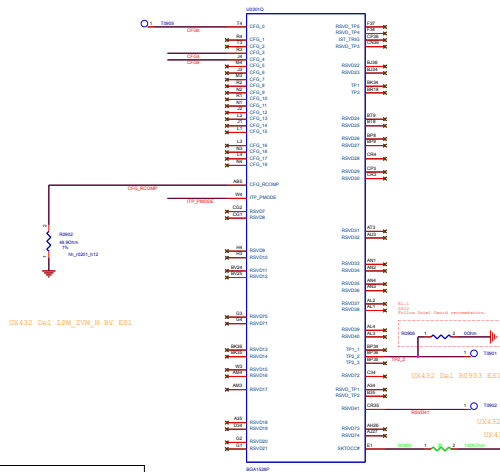




Table 6-7. Reset and Miscellaneous Signals (Sheet 1 of 2)

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
	<p><b>Configuration Signals:</b> The CFG signals have a default value of "1" if not terminated on the board. Refer to the appropriate Platform Design Guide for pull-down recommendations when a logic low is desired.</p> <p>Intel recommends placing test points on the board for CFG pins.</p> <ul style="list-style-type: none"> <li>• <b>CFG[0]:</b> Stall reset sequence after PCI/PLX lock until de-asserted.               <ul style="list-style-type: none"> <li>= 1 = (Default) Normal operation; No stall.</li> <li>= 0 = Stall.</li> </ul> </li> <li>• <b>CFG[1]:</b> Reserved configuration lane.</li> <li>• <b>CFG[2]:</b> PCI Express® State <math>\times 16</math> Lane Numbering Reversed.               <ul style="list-style-type: none"> <li>= 1 = Normal operation</li> <li>= 0 = Lane numbers reversed.</li> </ul> </li> <li>• <b>CFG[3]:</b> Reserved configuration lane.</li> <li>• <b>CFG[4]:</b> ASP enable.               <ul style="list-style-type: none"> <li>= 1 = Enabled</li> <li>= 0 = Disabled.</li> </ul> </li> <li>• <b>CFG[6:5]:</b> PCI Express® Bifurcation               <ul style="list-style-type: none"> <li>= 00 = 1 x16, 2 x4 PCI Express®</li> <li>= 01 = reserved</li> <li>= 10 = 2 x16 PCI Express®</li> <li>= 11 = 1 x16 PCI Express®</li> </ul> </li> <li>• <b>CFG[7]:</b> PEG Training               <ul style="list-style-type: none"> <li>= 1 = (Default) PEG Train immediately following RESET# de-assertion.</li> <li>= 0 = PEG Wait for BIOS for training.</li> </ul> </li> <li>• <b>CFG[19:8]:</b> Reserved configuration lanes.</li> </ul>				
CFG[19:0]		1	QTL	SE	All Processor Lines; CFG[2] - CFG[5] and CFG[7] are relevant for H and S-Processor Line only and test point may be placed on the board for them.
CFG_RESET#	<b>Configuration Resistance Compensation</b>	N/A	N/A	SE	All Processor Lines
CFG_P0PDRCOMP	<b>PD0P0 Resistance Compensation</b>	N/A	N/A	SE	S-Processor Line
RESET#	Platform Reset pin driven by the PCH.	1	CHOS	SE	H and S-Processor Line
PROC_SELECT#	<b>Processor Select:</b> This pin is for compatibility with future platforms; it should be unconnected for this processor.			N/A	H and S-Processor Line
PROC_TRIGEN	Debug pin. Refer to the appropriate Platform Design Guide for implementation details (See Related Documents section).	1	CHOS	SE	H and S-Processor Line

TP for Boundary Scan Test



	1	0	NOTE
CFG4	DISABLE	ENABLE	#0P ENABLE



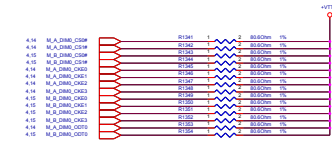
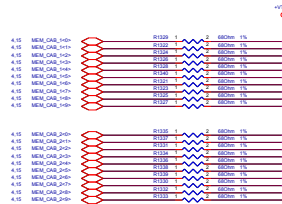
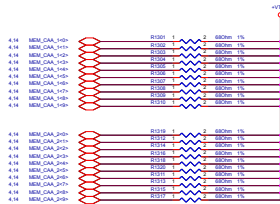


Table 11-2. Decoupling Requirements for Coffee Lake U Processor (Sheet 1 of 4)

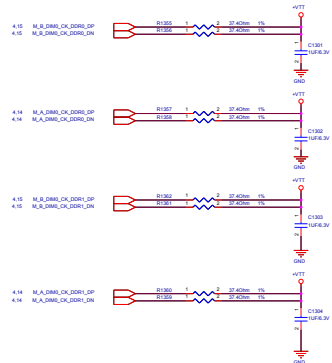
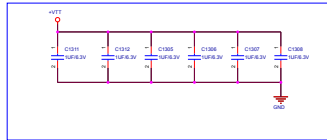
Domain	Backside cap	Primary side cap	Placement guideline
Vcc	35x 1uF 0201		Refer to diagram in Note 3 below for placement recommendations of 0201 caps
	7x 10uF 0402		
	9x 22uF 0603		
		8x 10uF 0402	Place as close to the package as possible
		5x 47uF 0805	
		4x 47uF 0805	Placeholder Only

+VCCCORE DeCap  
0201 1uF/6.3V XSR h14 \*30  
0402 4.7uF/6.3V XSR h13 \* 18

<b>ASUS</b>		Project Name	Rev
		UX432	R1.0
Title : CPU_POWER_CAP			
Size	Dept. : ASUS/NA COMPUTER INC.	Engineer: Tony1 chang	
Date: Wednesday, July 16, 2014	Drawn	by	of 100



Close to LPDDR3 t ermination n resistance (0402 siz e)



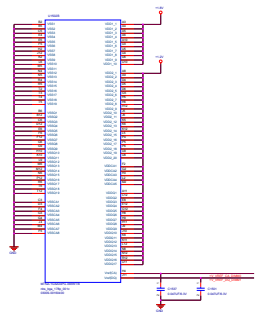
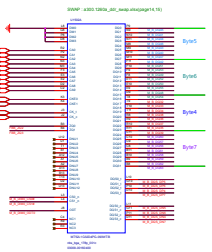
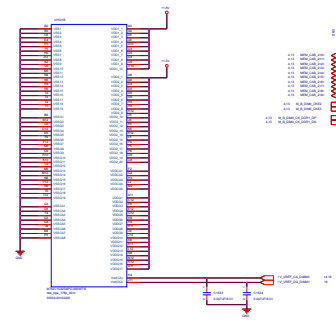
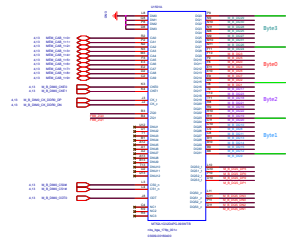
Contract Name:

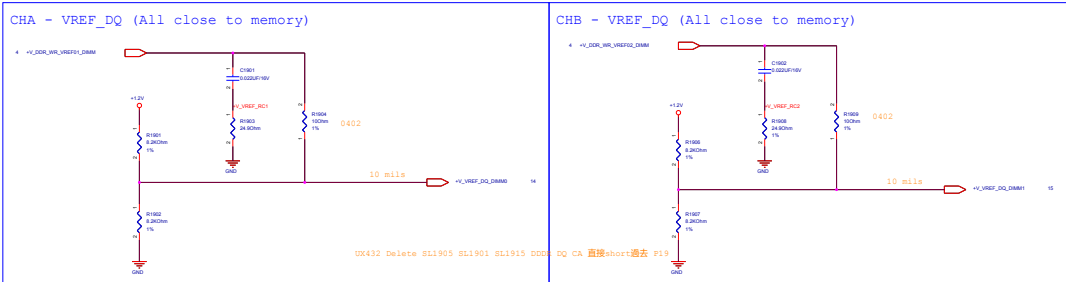
ASUS		Project Name	Rev
Title : LPDDR3_TERMINATION		UXX4.3.2	01.0
Drawn	Dept.: N01000022	Engineer: Tony1_chang	
Date: Wednesday, July 15, 2015	Drawn	1.3	of 152





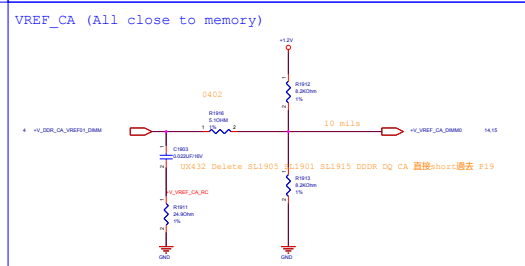
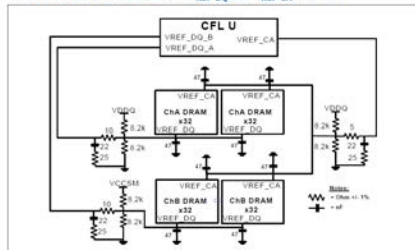
EPIDA & Samsung suggest 240 1k ohm  
Intel suggest 243 1k ohm





Power plan:1.2V

Figure 4-1. CFL U LPDDR3 x32 Memory Down  $V_{REF\_DQ}$  and  $V_{REF\_CA}$  Overview

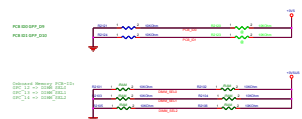


\*Variant Name:

Project Name		Rev
Title : LPDDR3 CA_DQ VREF		01.0
Size	Dept: HW/ROSE2	Engineer: Tony1_chang
Date: Wednesday, July 15, 2015	Sheet	19 of 102



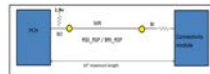
Main Board



	2133	2133	2133	2133
	Samung 5GB	Microon 5GB	Samung 16GB	Microon 16GB
SDMM_HL0	L A2101	L A2101	L A2101	L A2101
SDMM_HL1	L A2103	M A2104	L A2103	M A2104
SDMM_HL2	L A2105	L A2105	M A2104	M A2104

```
Samung@194: ~$ x32 1402(808) 03009-0001200 LPOB 2133 912M*32 FPGAL78 QD SAMUNG/K4E6K04BC-ECOC
Samung@194: ~$ x32 3202(1608) 30009-0016070 LPOB 2133 0324M*32 FPGAL78 QD SAMUNG/K4E6K04BC-ECOC
Micron@194: ~$ x32 1602(808) 03009-0003900 LPOB 2133 912M*32 FPGAL78 QD MICRON/MT9214120320209P-093 MT-9
Micron@194: ~$ x32 3202(1608) 30009-0016040 LPOB 2133 0324M*32 FPGAL78 QD MICRON/MT9214120320209P-093 MT-9
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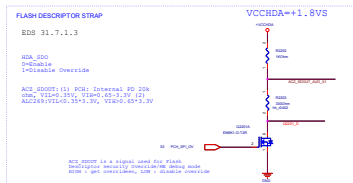
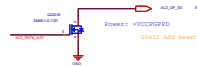
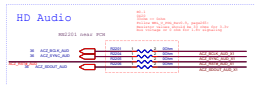
SOC	Configuration	XTAL Input Source	XTAL Input Pin1 [XTAL_IN1]	XTAL_IN12	SOC clock source
PLC	CM0 in No Clock Sharing Mode	Decomposed Pulled up internally	Depends on the frequency of the SOC clock. For 24 MHz, pulled up for 20 k $\Omega$ and down for 20 k $\Omega$ .	Pulled down by CM0 IN12_P1 pin	SOC crystal oscillator A 24-M or 48-MHz crystal should be connected at XTAL_IN1 and XTAL_IN12
	Discrete in No Clock Sharing Mode	Decomposed Pulled up internally	Default is 20-k $\Omega$ for pull-up and disconnected	Pulled up internally and 20 k $\Omega$ by CM0 IN12_P1 pin	
	CM0 in Clock Sharing Mode	Connected to Pull-down resistor	Decomposed Pulled down internally. Clock sharing can only work with 30-k $\Omega$ clock divider	Pulled down by CM0 IN12_P1 pin	CM0 30-k $\Omega$ clock tied back to CLKIN. XTAL_IN12 pin (single-ended)



● 曹明华, 等.  
● 曹明华, 等.  
● 曹明华, 等.  
● 曹明华, 等.



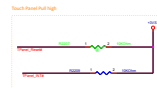
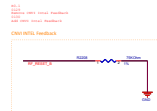
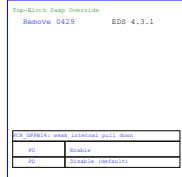
Project Name		ASUS
Title :		CPQ_CFG.RSV0.GND
Dept.:	ASUSTek COMPUTER INC.	Engineer: Tonyt_chang



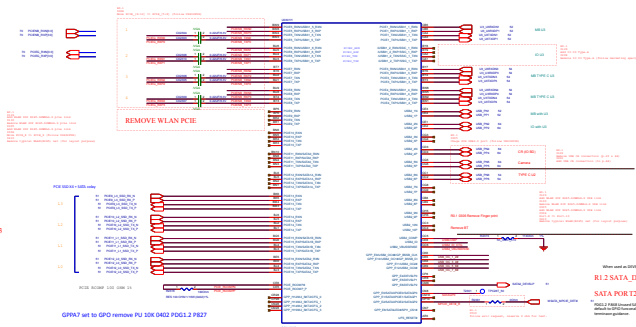
DESIGN TO enable flash descriptor memory override, this  
signal should be pulled up to VCCCHDA through a 1  
kΩ to 10 kΩ 40k resistor.



U432 Add PDS Figure 7-31 R02 33 ohm C2 27 PF







\*When used as DFFVUP, no external pull-up or pull-down termination is required from LSS1. Not DFFVUP.

## R1.2 SATA DEVSLP change to DEVSLP2

SATA PORT 2 0323

FIGURE 2.3.2: **FALSE** Unused GPIO pins can be left as no connect and need to be default to GPIO functionality, refer to an unused GPIO for terminations guidance.







Table 10.3. WPA-6 Subsample  $\chi^2$  (df=4) (all  $\chi^2$   $\geq 10.0$ )

Country	Year	Population (millions)	Per 1,000 live births	Per 1,000 live births	Per 1,000 live births	Per 1,000 live births
			1990	2000	2010	2015
Algeria	2015	3.5	12.0	12.0	12.0	12.0
Algeria	2010	3.5	12.0	12.0	12.0	12.0
Algeria	2005	3.5	12.0	12.0	12.0	12.0
Algeria	2000	3.5	12.0	12.0	12.0	12.0
Algeria	1995	3.5	12.0	12.0	12.0	12.0
Algeria	1990	3.5	12.0	12.0	12.0	12.0
Algeria	1985	3.5	12.0	12.0	12.0	12.0
Algeria	1980	3.5	12.0	12.0	12.0	12.0
Algeria	1975	3.5	12.0	12.0	12.0	12.0
Algeria	1970	3.5	12.0	12.0	12.0	12.0
Algeria	1965	3.5	12.0	12.0	12.0	12.0
Algeria	1960	3.5	12.0	12.0	12.0	12.0
Algeria	1955	3.5	12.0	12.0	12.0	12.0
Algeria	1950	3.5	12.0	12.0	12.0	12.0
Algeria	1945	3.5	12.0	12.0	12.0	12.0
Algeria	1940	3.5	12.0	12.0	12.0	12.0
Algeria	1935	3.5	12.0	12.0	12.0	12.0
Algeria	1930	3.5	12.0	12.0	12.0	12.0
Algeria	1925	3.5	12.0	12.0	12.0	12.0
Algeria	1920	3.5	12.0	12.0	12.0	12.0
Algeria	1915	3.5	12.0	12.0	12.0	12.0
Algeria	1910	3.5	12.0	12.0	12.0	12.0
Algeria	1905	3.5	12.0	12.0	12.0	12.0
Algeria	1900	3.5	12.0	12.0	12.0	12.0
Algeria	1895	3.5	12.0	12.0	12.0	12.0
Algeria	1890	3.5	12.0	12.0	12.0	12.0
Algeria	1885	3.5	12.0	12.0	12.0	12.0
Algeria	1880	3.5	12.0	12.0	12.0	12.0
Algeria	1875	3.5	12.0	12.0	12.0	12.0
Algeria	1870	3.5	12.0	12.0	12.0	12.0
Algeria	1865	3.5	12.0	12.0	12.0	12.0
Algeria	1860	3.5	12.0	12.0	12.0	12.0
Algeria	1855	3.5	12.0	12.0	12.0	12.0
Algeria	1850	3.5	12.0	12.0	12.0	12.0
Algeria	1845	3.5	12.0	12.0	12.0	12.0
Algeria	1840	3.5	12.0	12.0	12.0	12.0
Algeria	1835	3.5	12.0	12.0	12.0	12.0
Algeria	1830	3.5	12.0	12.0	12.0	12.0
Algeria	1825	3.5	12.0	12.0	12.0	12.0
Algeria	1820	3.5	12.0	12.0	12.0	12.0
Algeria	1815	3.5	12.0	12.0	12.0	12.0
Algeria	1810	3.5	12.0	12.0	12.0	12.0
Algeria	1805	3.5	12.0	12.0	12.0	12.0
Algeria	1800	3.5	12.0	12.0	12.0	12.0
Algeria	1795	3.5	12.0	12.0	12.0	12.0
Algeria	1790	3.5	12.0	12.0	12.0	12.0
Algeria	1785	3.5	12.0	12.0	12.0	12.0
Algeria	1780	3.5	12.0	12.0	12.0	12.0
Algeria	1775	3.5	12.0	12.0	12.0	12.0
Algeria	1770	3.5	12.0	12.0	12.0	12.0
Algeria	1765	3.5	12.0	12.0	12.0	12.0
Algeria	1760	3.5	12.0	12.0	12.0	12.0
Algeria	1755	3.5	12.0	12.0	12.0	12.0
Algeria	1750	3.5	12.0	12.0	12.0	12.0
Algeria	1745	3.5	12.0	12.0	12.0	12.0
Algeria	1740	3.5	12.0	12.0	12.0	12.0
Algeria	1735	3.5	12.0	12.0	12.0	12.0
Algeria	1730	3.5	12.0	12.0	12.0	12.0
Algeria	1725	3.5	12.0	12.0	12.0	

VIEWING SPOT

**Deep In Well:** 1.0V: This rail is generated by an on die DSW low dropout (LDO) linear regulator to supply DSW core logic. Board needs to connect 0.1µF capacitor to this rail and power should NOT be driven from the board.

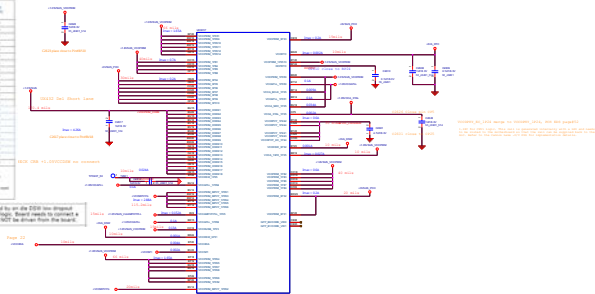
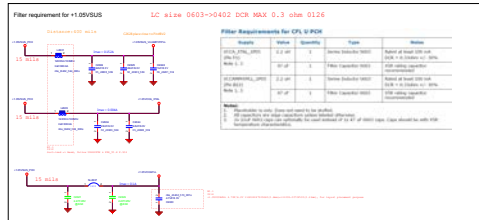
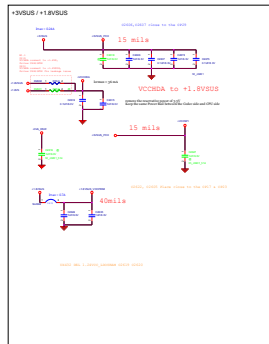


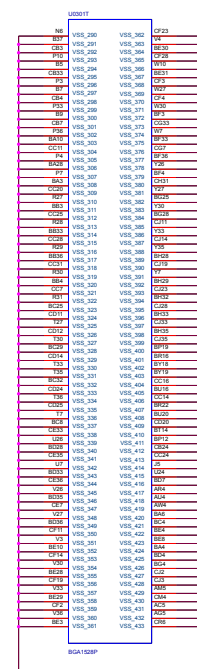
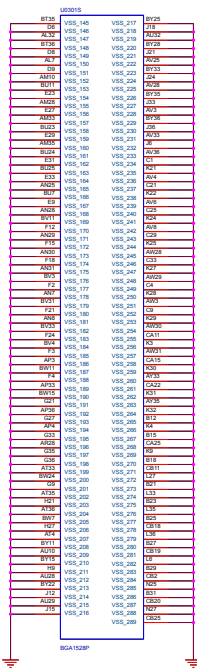
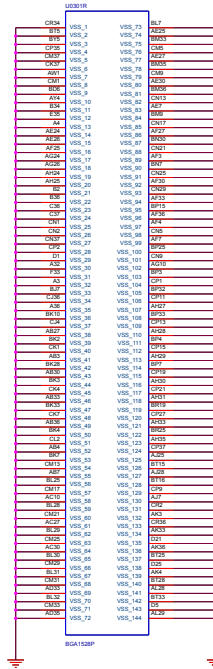
Table 1-1-5: Decoupling and Power Connection Requirements for QFN &amp; PFM (Sheet 1 of 2)

Year	Area	Number of inhabitants	Number of inhabitants in 2000	Number of inhabitants in 2005	Number of inhabitants in 2010	Number of inhabitants in 2015
2000						
2001	1000000	1000000	1000000	1000000	1000000	1000000
2002	1000000	1000000	1000000	1000000	1000000	1000000
2003	1000000	1000000	1000000	1000000	1000000	1000000
2004	1000000	1000000	1000000	1000000	1000000	1000000
2005	1000000	1000000	1000000	1000000	1000000	1000000
2006	1000000	1000000	1000000	1000000	1000000	1000000
2007	1000000	1000000	1000000	1000000	1000000	1000000
2008	1000000	1000000	1000000	1000000	1000000	1000000
2009	1000000	1000000	1000000	1000000	1000000	1000000
2010	1000000	1000000	1000000	1000000	1000000	1000000
2011	1000000	1000000	1000000	1000000	1000000	1000000
2012	1000000	1000000	1000000	1000000	1000000	1000000
2013	1000000	1000000	1000000	1000000	1000000	1000000
2014	1000000	1000000	1000000	1000000	1000000	1000000
2015	1000000	1000000	1000000	1000000	1000000	1000000
2016	1000000	1000000	1000000	1000000	1000000	1000000
2017	1000000	1000000	1000000	1000000	1000000	1000000
2018	1000000	1000000	1000000	1000000	1000000	1000000
2019	1000000	1000000	1000000	1000000	1000000	1000000
2020	1000000	1000000	1000000	1000000	1000000	1000000

Table 12 E. Strapping and Power Connection Requirements for DPs, 0 PCB (Sheet 2 of 2)

Case	Year	Study Design	Country	Sex	Age (years)	Prevalence (%)	Reference
1	1978-1980	Case-control	USA	Male	15-64	1.0	[10]
2	1978-1980	Case-control	USA	Male	15-64	1.0	[10]
3	1978-1980	Case-control	USA	Male	15-64	1.0	[10]
4	1978-1980	Case-control	USA	Male	15-64	1.0	[10]
5	1978-1980	Case-control	USA	Male	15-64	1.0	[10]
6	1978-1980	Case-control	USA	Male	15-64	1.0	[10]
7	1978-1980	Case-control	USA	Male	15-64	1.0	[10]
8	1978-1980	Case-control	USA	Male	15-64	1.0	[10]
9	1978-1980	Case-control	USA	Male	15-64	1.0	[10]
10	1978-1980	Case-control	USA	Male	15-64	1.0	[10]

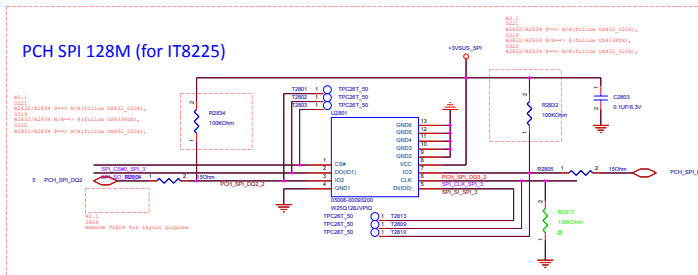
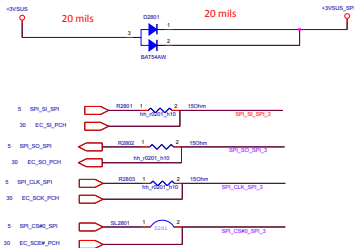




-Variant Name-

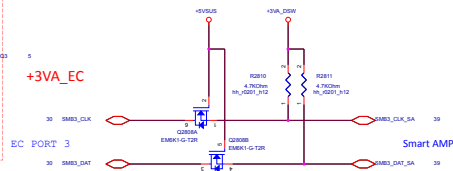
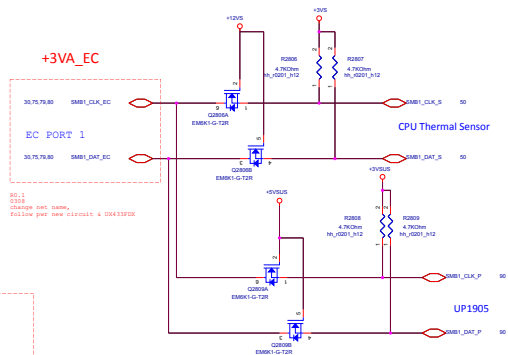
ASUS Project Name		Rev
Title : CPU_PCH_POEWR_GND		Rev. 1
Size	Dept. : ASUS&W COMPUTER INC.	Engineer : Tony1_chang
Date : Wednesday, July 18, 2018	Sheet	27 of 100

## System Management Interface



MS.1  
0409  
02801 05006-0009000 => 05006-0009200, follow WX4229WK.

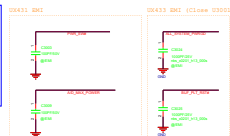
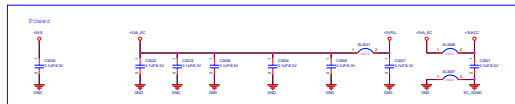
2nd : 05006-00093700  
main : 05006-00093200



```
EC 8995
Only 3V Torrence
GPR[0,1,2,3,4,5,6]
GPR[3,4,5,6,7]
GPD[0,4,6,7]
GRE[4]
GPF[6,7]
GPR[7]
GRT[0:7]
GPJ[0:7]

Can be adjusted to
Open-Drain for port:

GPAD-GPA3
GPBD-GPB7
GPCC-GPC7
GPED-GPE7
GPF0-GPF7
GPFD-GPFD6
GPJ0-GPJ5
```



```

90.1
C3023
246 ENG CAP C3024/C3025 reserve
-0.000 000000

```

ITE Version	ASUS P/E
IT8225VG-128/CX	06037-00240300

OT16  
disconnect PWRLOCK SC#, dallas  
SC posting guide V173

\_\_\_\_\_

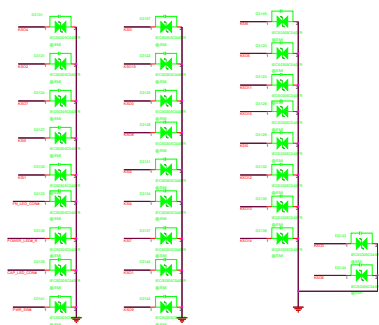
### Model 3

Follow your new friend

UX432 Del CHG FULL LED# CHG LED# pull high @R3021 @R3022 V<sub>bus</sub> e n Pulldown @R3019 P30 省空

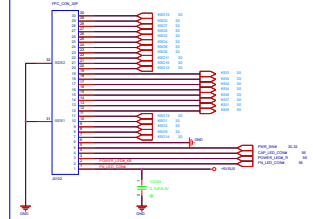
LX432 Delete PM\_PWRBTN# pull high @R3015

UX432 Delete PCH\_SUS\_STAT# GPP\_A14 @R3090 GPJ3 CLK\_TPMPCI\_PCH R0502 ADD T0505 (UX390)



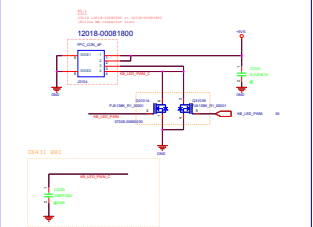
## Keyboard\_CON.

12018-00021100



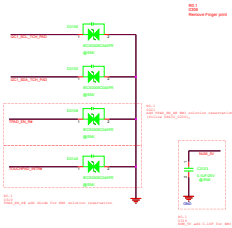
## BL\_CON.

12018-00081800

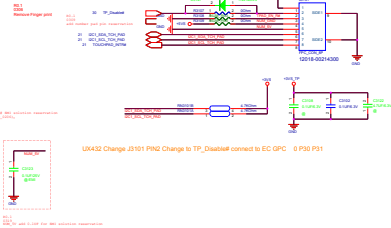


## Touch Pad

Finger Printer (USB)



## 同面cable !!



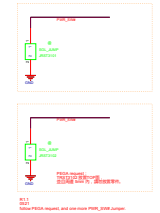
## SLAS / AN Sensor

Pin Assignment and Description		
Pin#	Signal	I/O Description
1	VCC	VCC, 5.3V +/-5% Power ripple: 100 mVpp max. Power sequence: See section 4.6.
2	WAKE	Not pin reserved in the connector for system wake-up
3	PS2_CLK	Not connected (Not reserve pin in the connector)
4	PS2_DATA	Not connected (Not reserve pin in the connector)
5	GND	Ground
6	PC_SDA	I/O PC data.
7	PC_SCL	I/O PC clock
8	INT	Indicates touchpad likes to send data to system (host)

PIN NO.	PIN DEFINE
1	VDD_3.3V
2	LTN_CLOSE (RESERVED)
3	GND
4	LED_VDD_5V
5	GND
6	I2C_SDA
7	I2C_SCL
8	/INT

Number pad pin define

## MOUSE



PS2 Mouse PS2C request, and use mouse PS2C\_SDA, PS2C\_SCL



## Main Board

②

②

```

#2.0
0713
Add #3214/#3213 - 0 ccm for testing purpose.

```

Age Group	Percentage
18-24	10%
25-34	15%
35-44	20%
45-54	25%
55-64	30%
65-74	35%
75-84	40%
85+	45%

Press PWR\_SW# 20s clear RTC for ASUS CSC request

Project Name

R1.0

Tony1\_chang

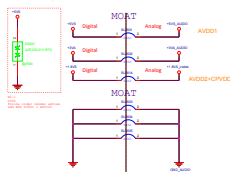
Size	Dept.: ASUS
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Engineer: Tony1\_chang

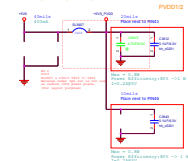
Date: Wednesday, July 18, 2018

Sheet 32 of 102

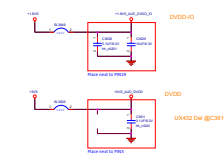
UX432 Def @D3801



UX432 Def @C3801 @C3802

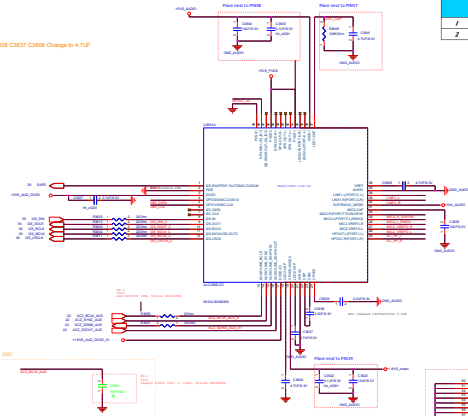


UX432 SL3601 SL3602 SL3614 SL3603 SL3604 SL3605 SL3640 SL3608 0 003 change to 0402

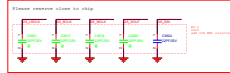
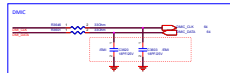
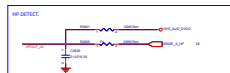
DVID10  
DVID0  
UX432 Def @C3810

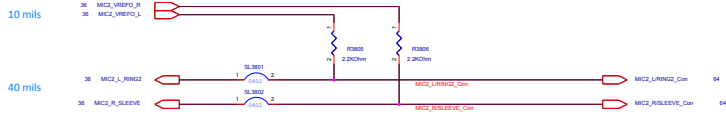
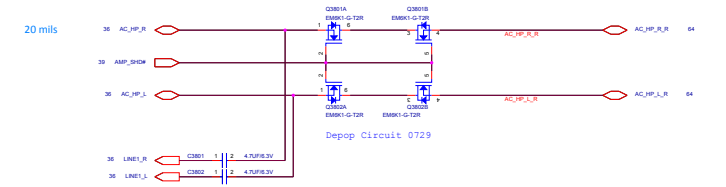
		DVID0 (1.8V/3.3V)	DVID10 (1.3V/3.3V)	AVDD1 (5V)	AVDD2+CPVDD (1.8V)	PYDD1/2 (5V)	Total Power
1	DVID0-1.8V, DVID10-1.3V	3.390	0.097	14.45	70.4	390	5503.14775
2	DVID0-3.3V, DVID10-3.3V	5.903	0.175	14.46	70.66	390	5610.375

UX432 C3841 C3808 C3837 C3806 Change to 4.7uF

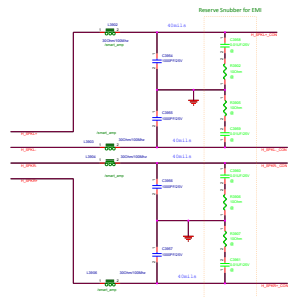
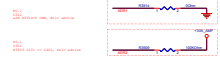
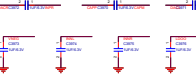
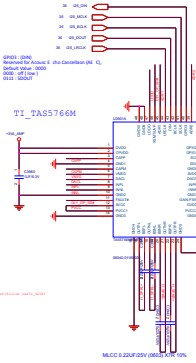
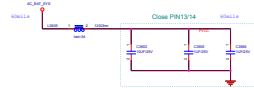
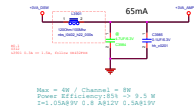
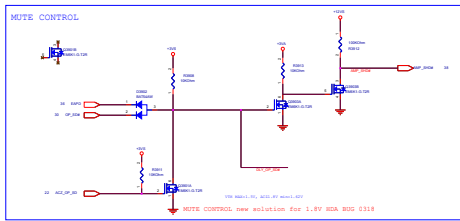


UX432 SMC

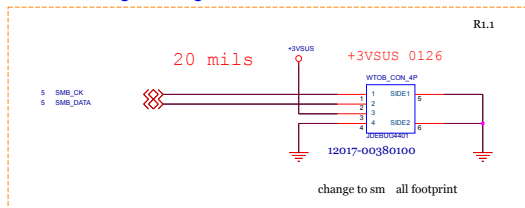




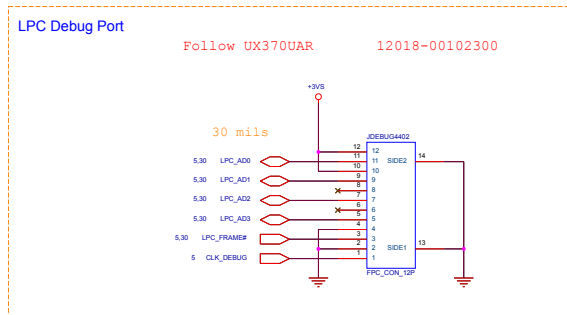
BT1.1  
Add main board audio Jack  
BT1.2  
move to 10 mil



## New Design Debug Port



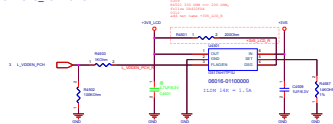
## LPC Debug Port



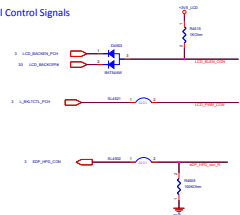
&lt;Variant Name&gt;

ASUS		Project Name	Rev
UX432			R1.0
Title : BUG_Debug			
Size	Dept.:	ASUSTek COMPUTER INC. Engineer:	Tony1_chang
A4			
Date: Wednesday, July 18, 2018		Sheet	44 of 100

LCD +3VS\_LCD Power



### Panel Control Signals



## LED AC BAT Power



## DMIC

Camera USB

### Touch Panel I2C Pull High

### Touch Reset Control

TPanel\_Report\_SW

## EDP Signals

UX432 Delete EDP 2 LANE EDP\_TXN2 EDP\_TXN3

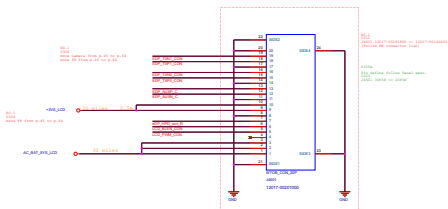


Figure 1: Schematic representation of the genetic circuit. The figure shows four panels (D2, D1, D0, CLK) illustrating the genetic circuit components and their interactions. Each panel shows a DNA strand with various genetic elements: a red arrow for the promoter, a blue box for the gene, and a green box for the output. The circuit is designed to produce a specific output (green box) based on the input (red arrow). The panels show the circuit's behavior under different conditions, with the output being 'ON' or 'OFF' depending on the input and the state of the circuit.

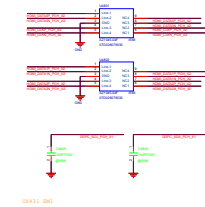
[illegible]

Pinout diagram of the 1202-00132100 connector. The diagram shows a 24-pin connector with pins numbered 1 to 24. Pins 1-12 are labeled with various signals: D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11. Pins 13-24 are labeled with various signals: D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, D23. A legend on the right lists the signals: D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, D23. A note at the bottom states: 'New connector, need to check pin defines.'

Segment	Stack-up	Wp (mm) <sup>2</sup>	Max Length (mm)	Max Length (mm)
Max Total Size			1.45 03/4	2.87 03/4

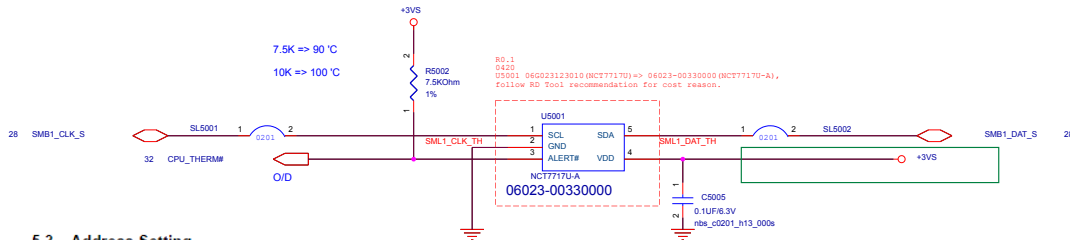
1. CPU's of 2.97 GHz supports only 32-bit (no 64-bit) for 32 and 64 bit integrally.
2. 12 only 32-bit for main body machine.
3. 32-bit is recommended, 64-bit is optional.
4. Available (32) system + 740 other 12-bit.
5. Max 4096 bits + 3 other.
6. The 3.50 supply should be 100-120 which will turn off to 1000 status.

$I_{ds} = 3.3 \times (470 + 50) \times 8 = 5.0 \text{mA}$   
 For under 1.65GHz



		Project Name		Date
		U3432		8/12
Title: HDMI-type D				
Site	Dept.	Engineer		
C	ASUS	Tony's_chang		
Date: Wednesday, July 15, 2015		Print	ok	ok

## CPU Sensor



### 5.3 Address Setting


NCT7717U I2C/SMBus address is 1001000xb (x is R/W bit).

### 5.6 ALERT# point hardware power-on setting (TBD)

The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin :

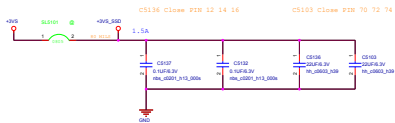
PULL-UP RESISTOR		TEMPERATURE (°C)
ALERT	2KΩ	75
	7.5KΩ	90
	10.5KΩ	100
	14KΩ	105
	18.7KΩ	110

<Variant Name>

		Title : FAN_Fan & Sensor	
ASUS		Engineer: Tony1_chang	
Size	Project Name	Rev	
Custom	UX432	R1.0	
Date:	Wednesday, July 18, 2016	Sheet	50 of 102



## SSD CONN.

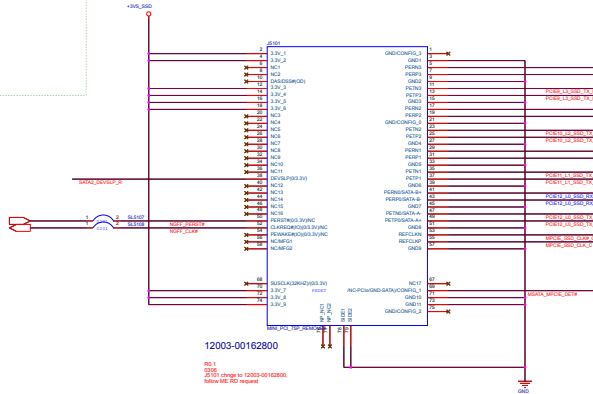


SATA DEVSPL.



```
Delete SATA2_DEVSLEP_R R5317 0 ohm ADD SL5102 直接short r5101 0ohm nonDEVSLEP P51
```

PCIE Wake-up.



UX432 Delete @R5103 @C5199 R5105 MSATA\_MPCIIE\_DET# (UX376)  
FULL HIGH PCN Side R2302



#### 36.3.2.4 AC Capacitor General Guidelines for M.2 SSD Storage Routing on SATA / PCI Express\* Multiplexed Ports

The following table summarizes the AC capacitor requirements on the motherboard when using the SATA/PCIe<sup>®</sup> multiplexed ports.

### Abstract

When SATA and PCIe® are mixed, always route according to SATA design guidelines. SATA does not support signal polarity reversal and does not support lane reversal.

Table 36-7. SATA / PCI Express® Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express <sup>®</sup> Gen 2 Only	PCI Express <sup>®</sup> Gen 3 Only	SATA Only	PCI Express <sup>®</sup> Gen 2/ SATA	PCI Express <sup>®</sup> Gen 3/ SATA
Processor 1a	100 nF	220 nF	20 nF	100 nF	220 nF
Processor 3a	None	None	10 nF <sup>2</sup>	None	None <sup>3</sup>



Maximum power consumption  
with both Wi-Fi and BT active  
WLAN: 3.3VS  $\rightarrow$  1050 mW  $\rightarrow$  320 mA  
BT : 3.3VS  $\rightarrow$  163mW  $\rightarrow$  50 mA  
Peak current=1.36A

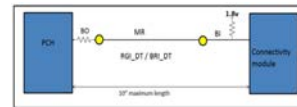
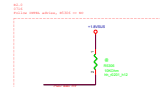
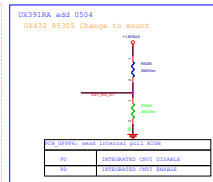
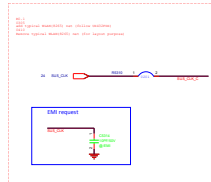
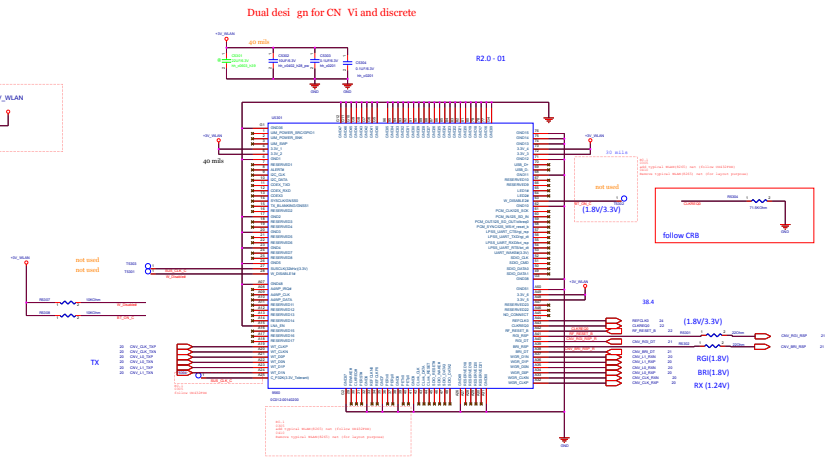
CFL&CN 1. Do not use clock sharing mode

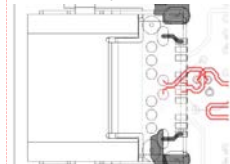
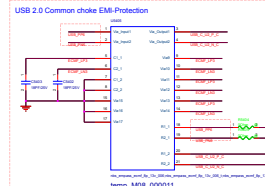
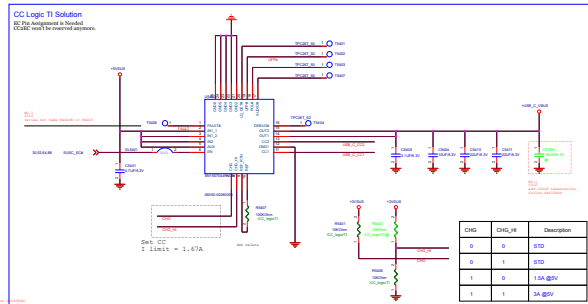
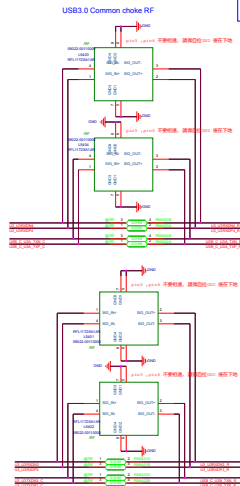
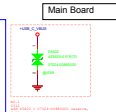
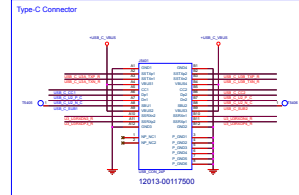
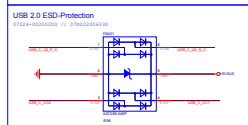
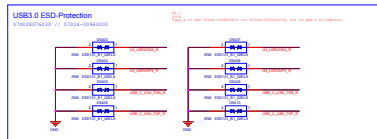
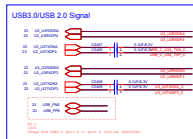


```

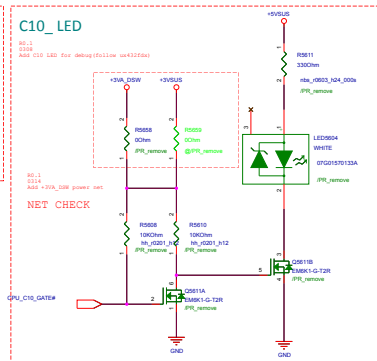
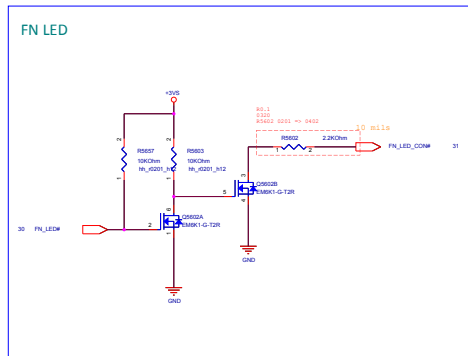
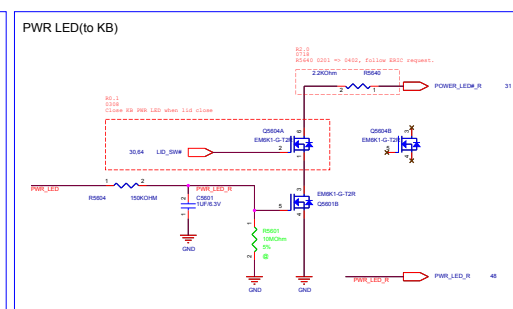
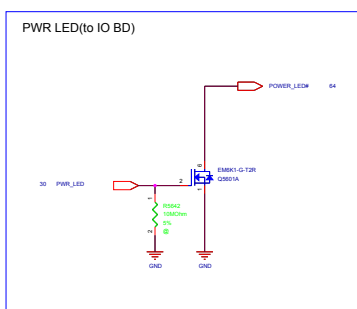
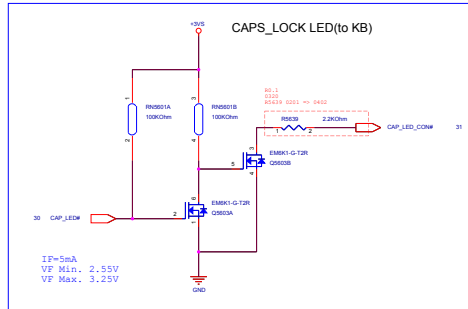
0011
0012
add wlan power gating switch, follow guidelines
0013
Remove wlan power gating switch

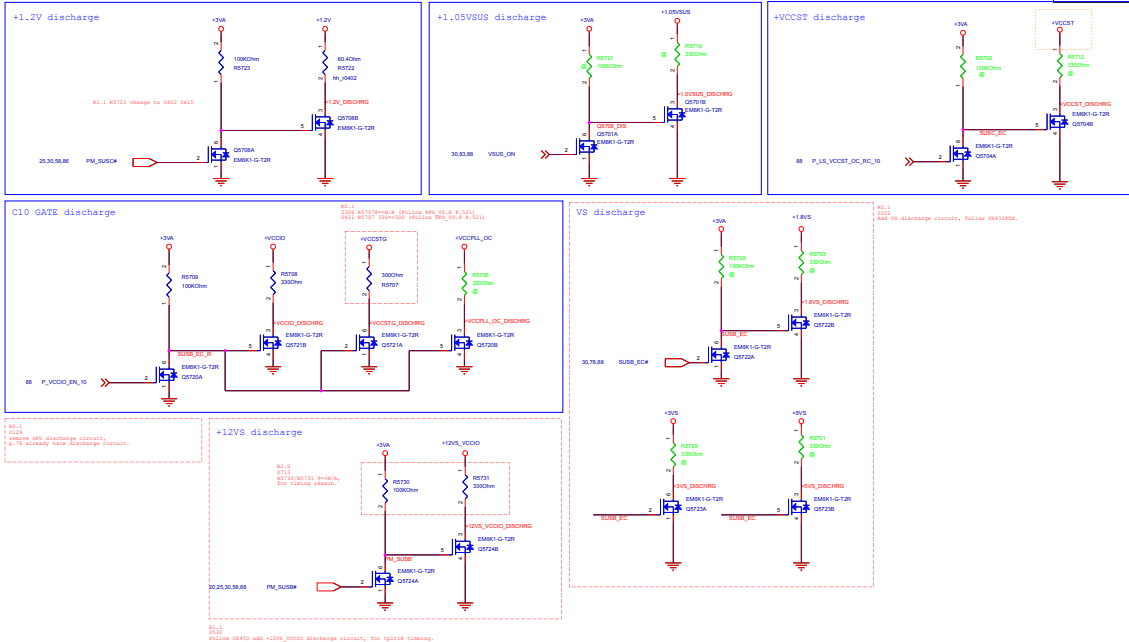
```





CHG	CHG_F8	Description
0	0	STD
0	1	STD
1	0	1.5A @5V
1	1	3A @5V

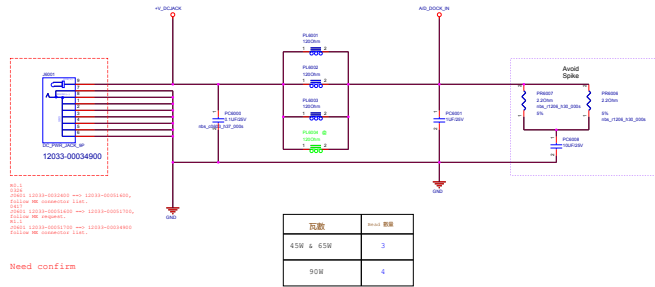




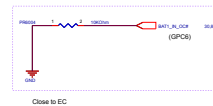
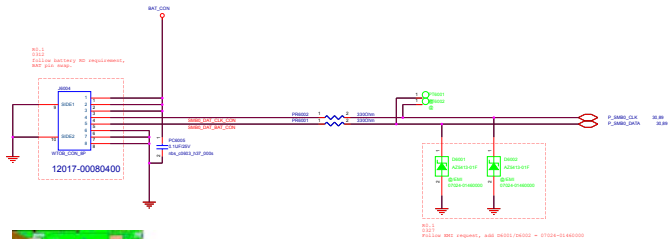
\*Variant Name\*

Project Name	UX432	Rev	R1.0
Title	DSG_Discharge		
Dept.	ASUSTek COMPUTER INC.	Engineer	Tony1_chang
Date	Wednesday, July 18, 2018	Sheet	57 of 100





## Battery Connector

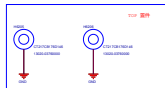




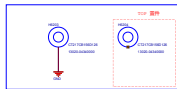
## CPU 13020-03760000



## GPU 13020-03760000



## FPC 13020-04340000

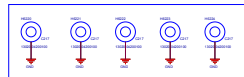


## Barcode for SMD



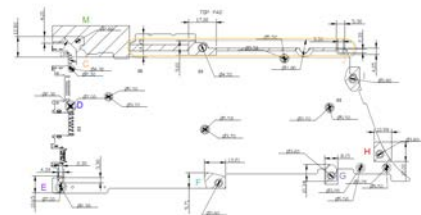
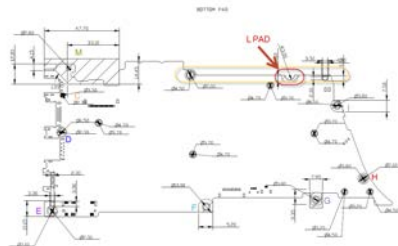
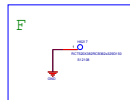
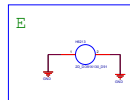
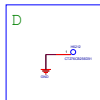
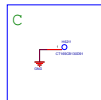
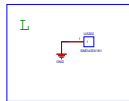
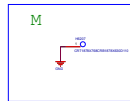
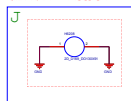
13020-04340000  
13020-04340000  
13020-04340000

## Support NUTS

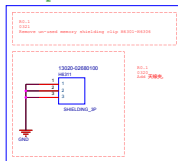


## ME Hole

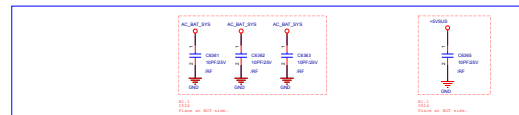
13020-04340000  
13020-04340000  
13020-04340000



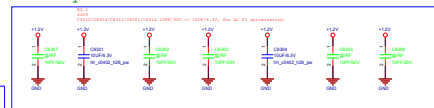
## Clip



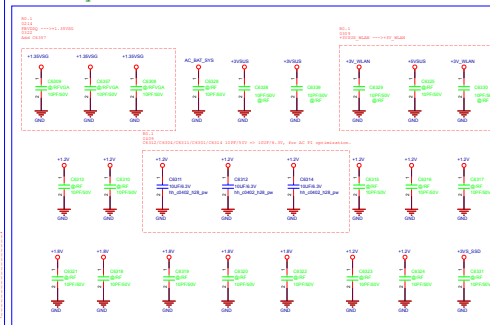
## RF request



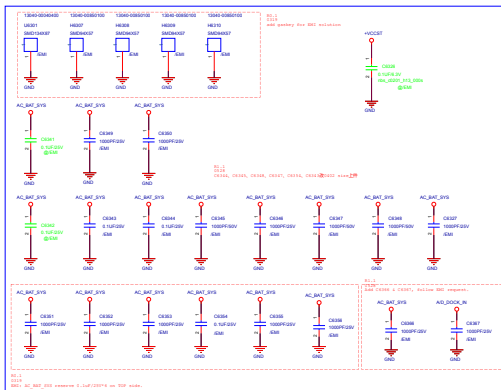
## RF request

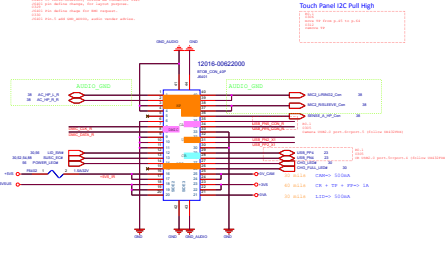
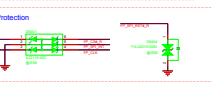
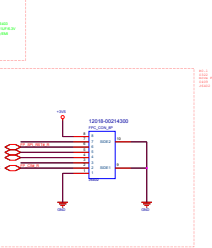
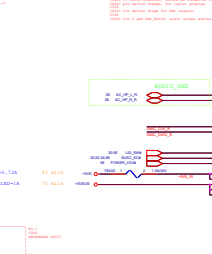
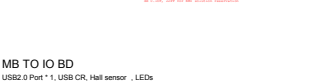
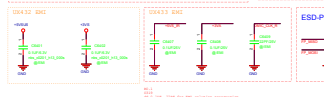
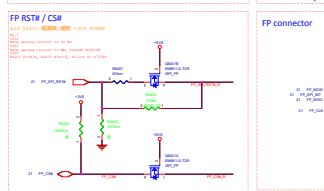
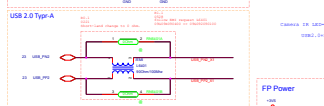
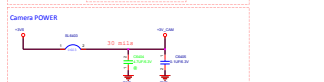
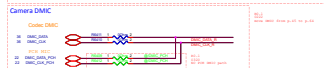
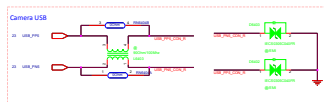


## RF request



## EMI request









## GPU MEMORY INTERFACE

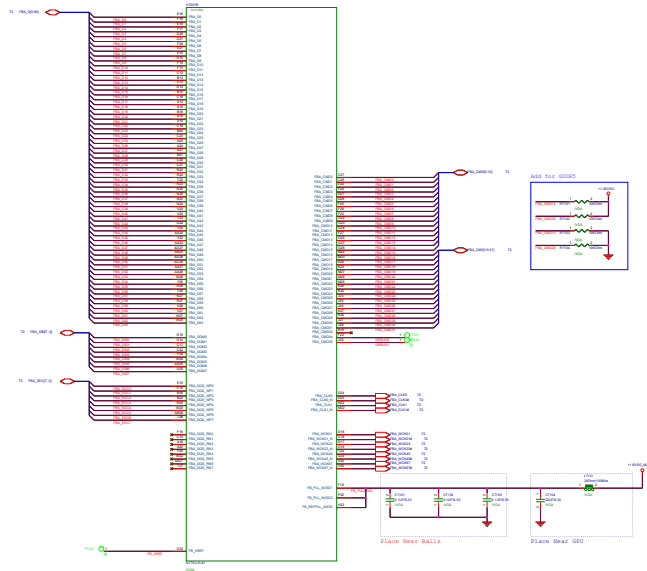
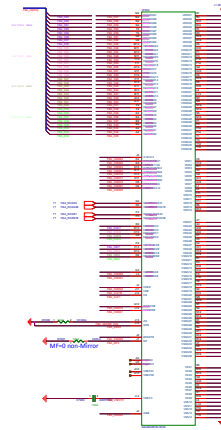


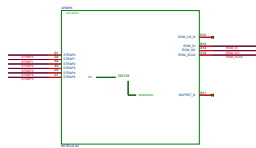
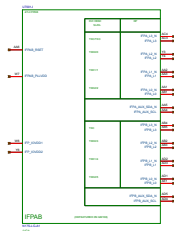
Table 9.5 GDDR5 Command Mapping (GB2C-64 packages)

Command Ball on GPU		DRAIN Signal Definition
For DRAIN(s) tied to DQ[31:0]	For DRAIN(s) tied to DQ[43:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A4_BA4
FBA_CMD3	FBA_CMD19	A5_BA5
FBA_CMD4	FBA_CMD20	A6_BA6
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A9_A10
FBA_CMD8	FBA_CMD24	A11_A12
FBA_CMD9	FBA_CMD25	A13_A14
FBA_CMD10	FBA_CMD26	A15_A16
FBA_CMD11	FBA_CMD27	A17_A18
FBA_CMD12	FBA_CMD28	A19_A20
FBA_CMD13	FBA_CMD29	A21_A22
FBA_CMD14	FBA_CMD30	A23_A24
FBA_CMD15	FBA_CMD31	A25_A26



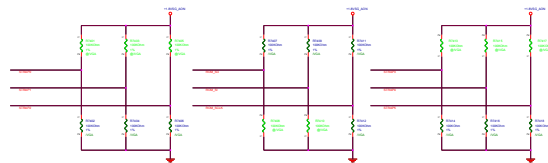
Command Ball on GPU		DHAP Sign Definition
For DRA001 to DQ031-1	For DRA001 to DQ031-12	
FBA_C000	FBA_C000	C3P
FBA_C001	FBA_C007	00_0A0
FBA_C002	FBA_C008	00_0B0
FBA_C003	FBA_C009	00_0C0
FBA_C004	FBA_C000	00_0D0
FBA_C005	FBA_C001	00_0E0
FBA_C006	FBA_C002	00_0F0
FBA_C007	FBA_C003	00_100
FBA_C008	FBA_C004	00_110
FBA_C009	FBA_C005	00_120
FBA_C0010	FBA_C006	00_130
FBA_C0011	FBA_C007	00_140
FBA_C0012	FBA_C008	00_150
FBA_C0013	FBA_C009	00_160
FBA_C0014	FBA_C000	00_170
FBA_C0015	FBA_C001	00_180





Row Index	Strap Pins (see Note)			Resulting SOR <sub>i</sub> _EXPOSED Enablements			
	SOR <sub>0</sub> _S0	SOR <sub>0</sub> _S1	SOR <sub>0</sub> _S2	SOR <sub>0</sub> _EXPOSED	SOR <sub>1</sub> _EXPOSED	SOR <sub>2</sub> _EXPOSED	SOR <sub>3</sub> _EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
0	H	H	H	disabled	disabled	disabled	disabled

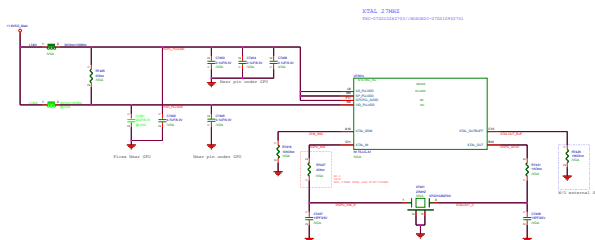
Strap Pins (see Note 1)			Functions Selected by This Strapping			
STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	STRAP5	STRAP6
L	L	L	L	L	L	L



Strap Pins (see Note)			RANGE <sub>0</sub> Setting Number
STRAP0	STRAP1	STRAP2	(see Memory RWL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
H	H	H	8 (0x0008)

Table 5. N175-LG GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code	Qual Pin	Status
8 Gb	256Mb/32	1.35V	SamSung	K4A803279B-HC25	5-die	0x0	7 Gbps	81/A	Full	Production ready
			SamSung	K4A803279B-HC25	5-die	0x0	8 Gbps	81/A	Full	Substitution allowed with wafer*
			Microon	MT11L125MA32HF-70-A	A-die	0x1	7 Gbps	81/A	Full	Production ready
			Microon	MT11L125MA32HF-80-A	A-die	0x1	8 Gbps	81/A	Full	Substitution allowed with wafer*
			Hynix	H5CG81248UR-R0C	A-die	0x2	7 Gbps	81/A	Full	Post production ready
			Hynix	H5CG81248UR-R4C	A-die	0x2	8 Gbps	81/A	Full	Substitution allowed with wafer*
			Microon	MT11L125MA32HF-70-B	B-die	0x1	7 Gbps	81/A	Full	Post production ready
			Microon	MT11L125MA32HF-80-B	B-die	0x1	8 Gbps	81/A	Full	Substitution allowed with wafer*





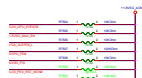
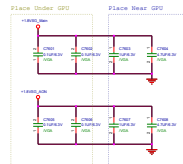
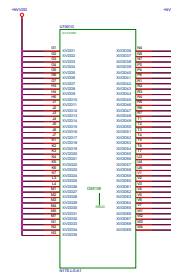
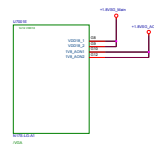
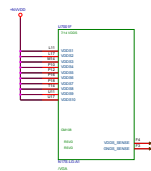
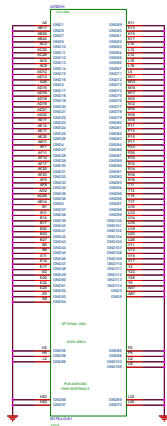


Table 14.1 GPIO Descriptions for GB2C-64 Packages

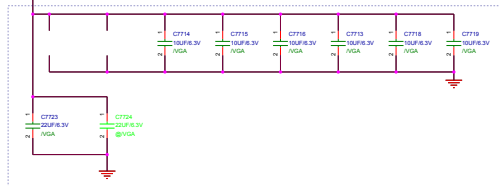
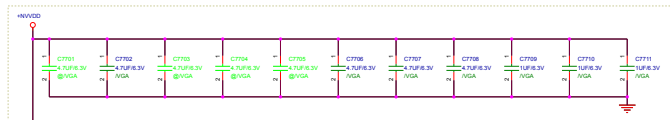
GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	HYVDD_P0IN	O	P0IN output to control HYVDD	0 to 10V I/O pin
GPIO1	GCGR_GCR_P0EN	O	P0 Enable for GC6 2.1	Open Drain
GPIO2	GCGR_GPIO_EVENT* WAKE*	I	GPIO wake signal for GC6 2.1	10 kΩ pull up to V1B_A0H, unless driven actively.
GPIO3	HYVDD_P0IN	I/O	P0IN output to control the HYVDD power supply	0 to 10V output
GPIO4	GCGR_V1B_M0EN	O	GPIO power sequencing for GC6 2.1	Open Drain 10 kΩ pull up to V1B_A0H
GPIO5	FIRM_LCK*	I	Active low FIRM lock	Open Drain 10 kΩ pull up to V1B_A0H
GPIO6	HYVDD_P0V* HYVDD_P0V	O	Power/Standby (see <a href="#">Section 44.3.3</a> )	10kΩ pull up to V1B_A0H to enable active power plane
GPIO7	LED_RL_P0IN	O	Power Switchback enable	100 kΩ pull down
GPIO8	MR_VDD_CTL	O	Memory Voltage Control	Pull-up to VDD to set the HYVDD power on voltage
GPIO9	THERM_ALERT*	I/O	Active-Low Thermal Alert	Open Drain 10 kΩ pull up to V1B_A0H
GPIO10	MR_VREF_CTL	O	Memory VREF Control	100 kΩ pull down

GPIQ Number	GPIQ Name	I/O	Functional Description	I/O Termination
GPIQ11	LED_VCO_Video_Power_Brake*	Q	Panel Power enable	100 kΩ pull-down
GPIQ12	PWR_LEVEL	A	AC power detect or power supply over-voltage input	100 kΩ pull-up to V1B_A0H
GPIQ13	LED_BLRK	O	LED Panel Backlight Enable	Panel Backlight Enable
GPIQ14	HPS_PPFA	I	Hot Plug Detect for PPFA	Inputted input. See Figure 14-3
GPIQ15	HPS_BFPE	I	Hot Plug Detect for BFPE	Inputted input. See Figure 14-3
GPIQ16	SPS_PCLK_RST_MON*	I	System side PCLK reset monitor	10 kΩ pull-up to V1B_A0H unless actively driven
GPIQ17	UNRES1	I/O		
GPIQ18	UNRES2	I/O		
GPIQ19	SD_Vision	O	SD Vision I/O signal	100 kΩ pull-down
GPIQ21	MEM_VIO_CTL	O	Frame Buffer VIO select	Open Drain; Pull-up pull-down to set the FBVIO2 to power-on output at boot up
GPIQ22	UNRES3	I/O		
GPIQ23	GCORE_GPIO_RST_HOLD*	O	GPU GCORE reset/control	Open Drain; Pull-up pull-up to signal VDD



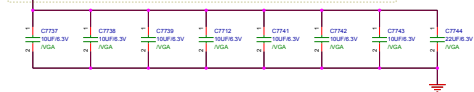
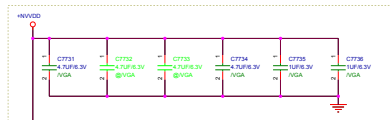
# NVDD POWER AND DECOUPLING

Place Under GPU

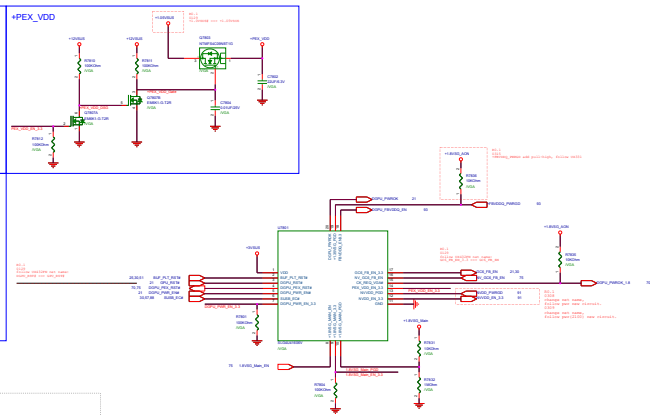
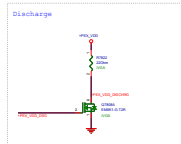
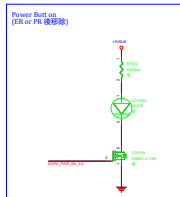
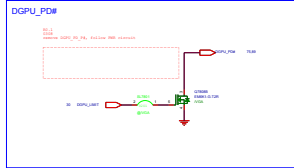
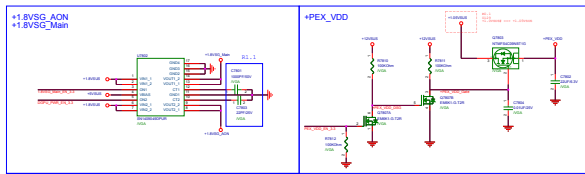


Place Near GPU

Place Under GPU

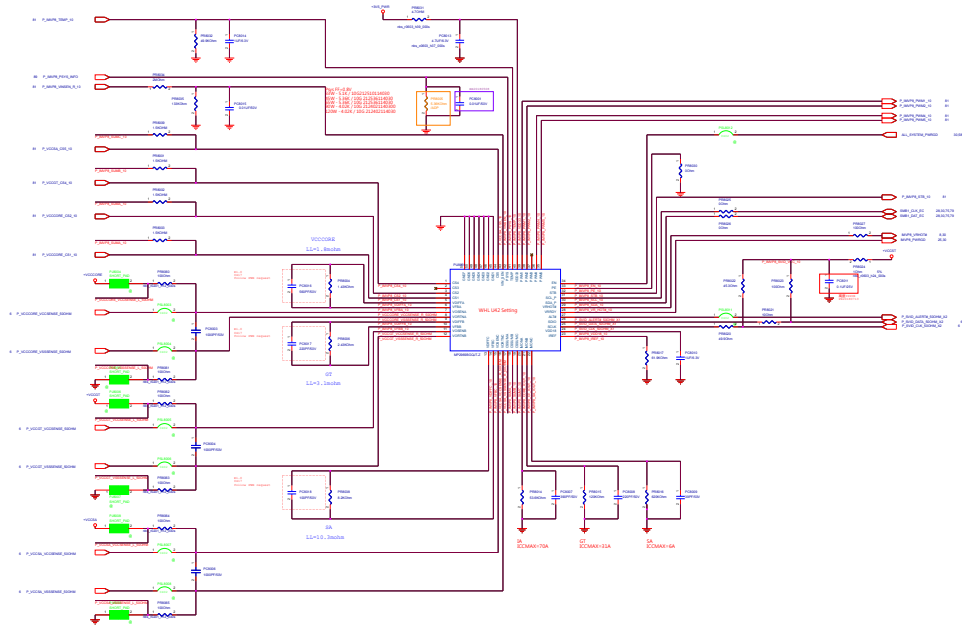


Place Near GPU

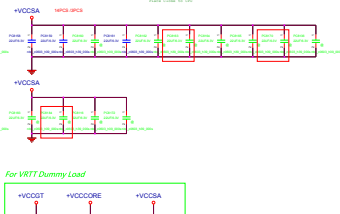
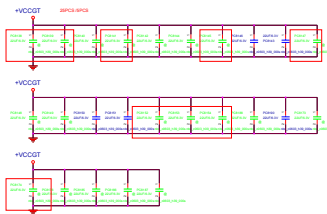
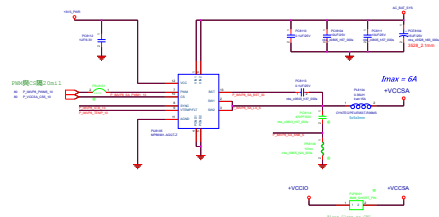
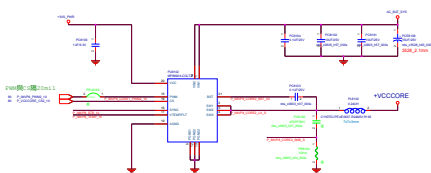
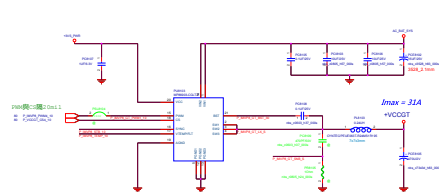
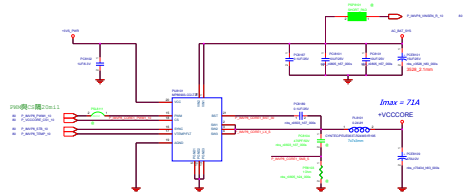




*WHL IMVP8 (1) Power [For CPU]*



WHL IMVP8 (2) Power [For CPU]

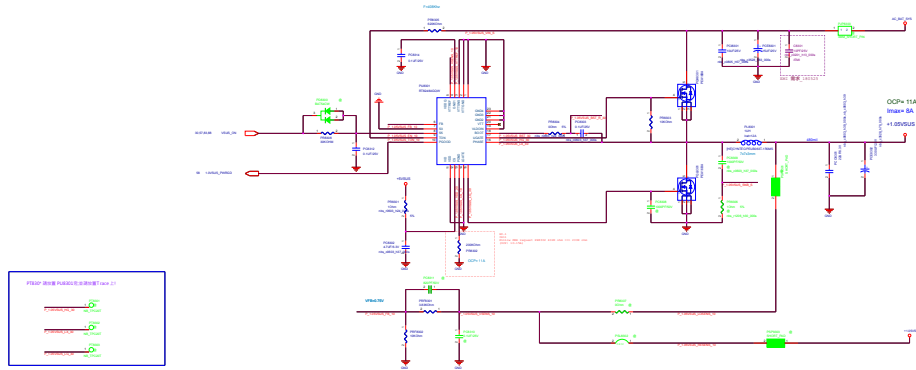


*For VRTT Dummy Load*

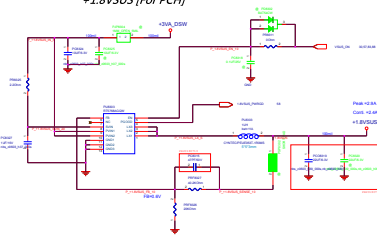


ASUS		Project Name	Rev
DESIGN_XP			Rev 01
Title: PIV, WYNDOLY LAKE G2			
Date	Dept: Mkt/Power Team	Engineer:	SS
Alt			

+1.05VSUS [For PCH]

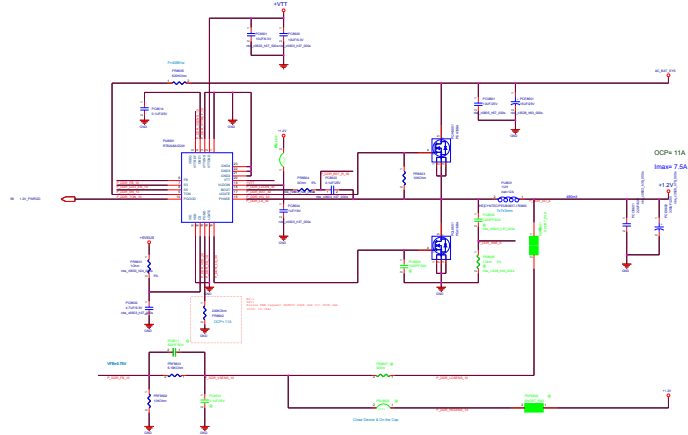
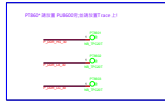
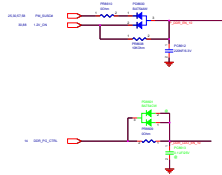


*+1.8VSUS [For PCH]*

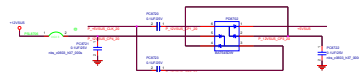
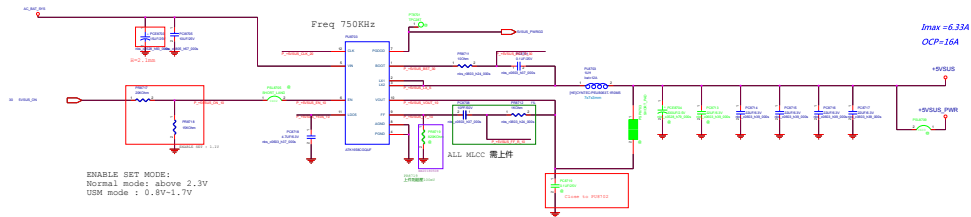
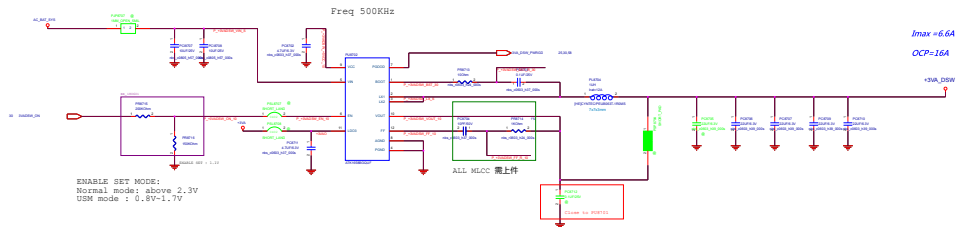




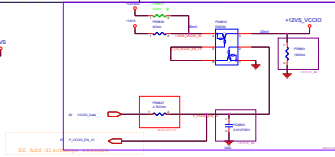
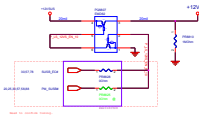
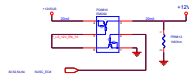
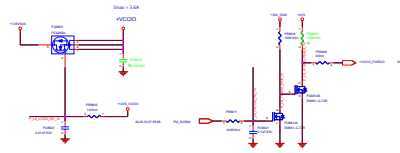
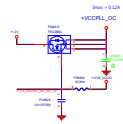
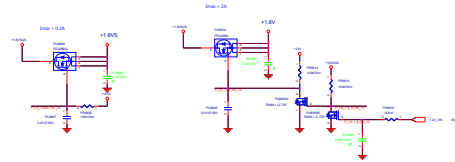
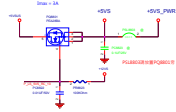
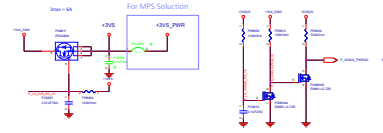
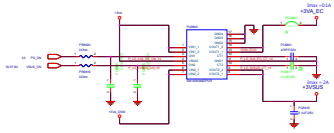
+1.2V / +VTT [For Memory]



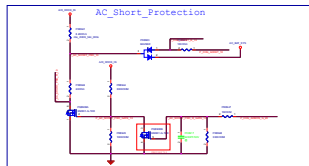
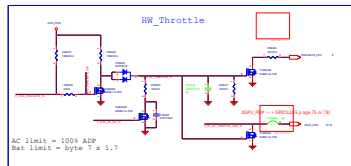
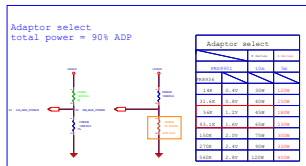
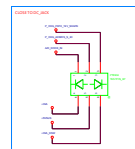
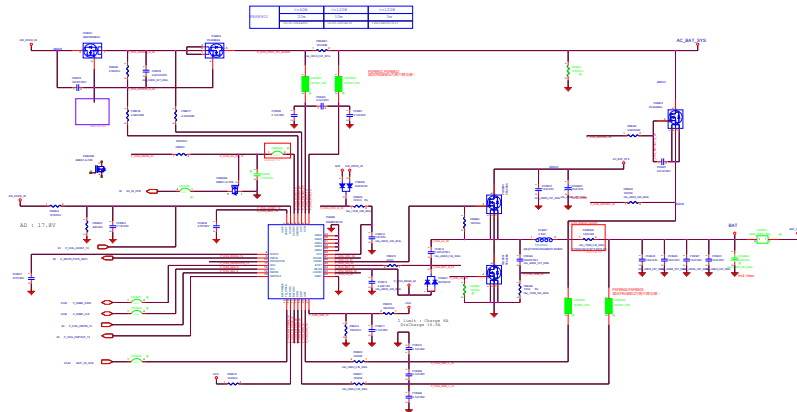
**+3VA\_DSW / +5VSUS [System Power]**



*Load Switch*

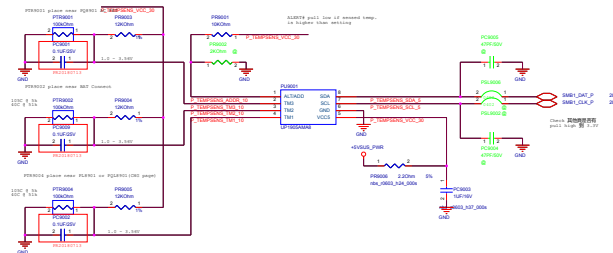


ASUS		Project Name:		U3633		Ver:		1.0	
Title:		PWR_LOAD_SWITCH							
Date:		Dept.:		ASUS		Engineer:		SS	
Date:		Wednesday, Aug 16, 2006		Time:		06		42	



Address	Se7E	Se7C	Se7A	Se7B	Se7D	Se7E	Se7F	Se7G
PR9003	10%	1.8%	2%	3.6%	3.9%	4.3%	5.1%	6%
PR9002	Open	8.2%	6.2%	6.8%	6.7%	3.6%	2.7%	2%

Address	SwD0	SwD1	SwD2	SwD3	SwD4	SwD5	SwD6
R/W	W	W	W	R	R	R	R
Function	Temp. alert threshold setting			Desired temp. data			bit 6 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert

[illegible]

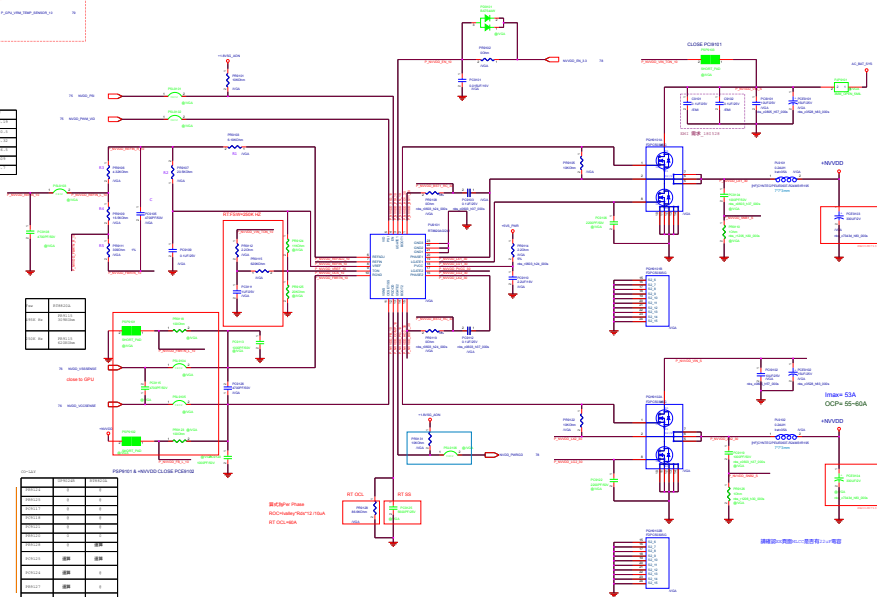


+NVVDD [For DGPU]



	20.6	20.7
$\beta_{11}$ (kN/m)	2.0	6.46
$\beta_{12}$ (kN/m)	2.0	20.5
$\beta_{13}$ (kN/m)	2	4.32
$\beta_{14}$ (kN/m)	1.6	16.5
$\beta_{15}$ (kN/m)	2	32.6
$\gamma$ (rad)	2.7	4.7

Year	2018-2021
1500K: Size	20-NG 1.5 30-NG 10mm
1500K: Size	20-NG 1.5 40-NG 10mm



型号	功率/W	频率/kHz	频率范围/kHz
PC9124	0	0	0
PC9125	0	0	0
PC9126	0	0	0
PC9127	0	0	0
PC9128	0	0	0
PC9129	0	0	0
PC9130	0	0	0
PC9131	0	0	0
PC9132	0	0	0
PC9133	0	0	0
PC9134	0	0	0
PC9135	0	0	0
PC9136	0	0	0
PC9137	0	0	0
PC9138	0	0	0
PC9139	0	0	0
PC9140	0	0	0
PC9141	0	0	0
PC9142	0	0	0
PC9143	0	0	0
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PC9147	0	0	0
PC9148	0	0	0
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PC9150	0	0	0
PC9151	0	0	0
PC9152	0	0	0
PC9153	0	0	0
PC9154	0	0	0
PC9155	0	0	0
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PC9159	0	0	0
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PC9162	0	0	0
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PC9165	0	0	0
PC9166	0	0	0
PC9167	0	0	0
PC9168	0	0	0
PC9169	0	0	0
PC9170	0	0	0
PC9171	0	0	0
PC9172	0	0	0
PC9173	0	0	0
PC9174	0	0	0
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PC9176	0	0	0
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PC9194	0	0	0
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PC9199	0	0	0

### 12PM FUNCTION

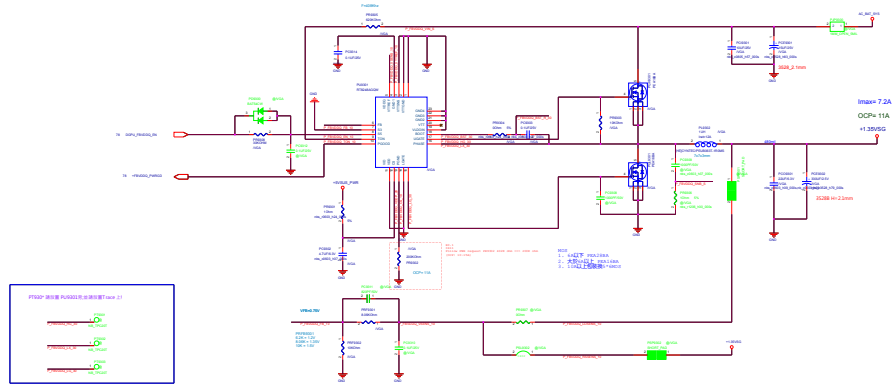
圖式39 Per Phase  
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RT 0.01584

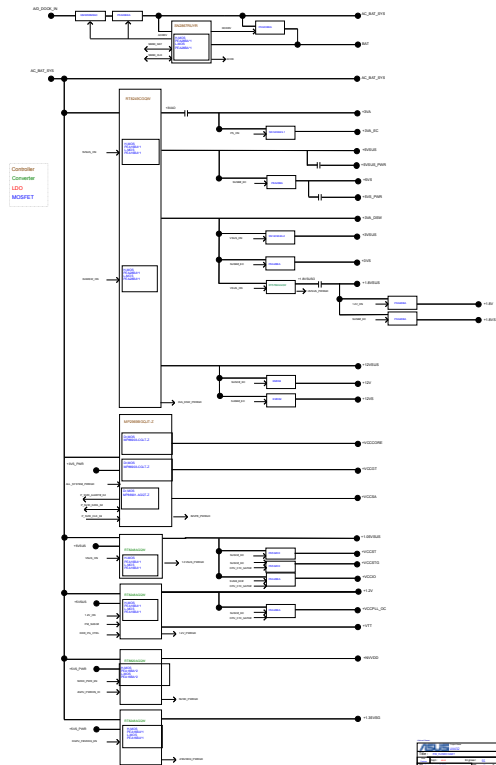
RT 29

PT910\* 請放置 Pu900 同: 並請放置 T race 上

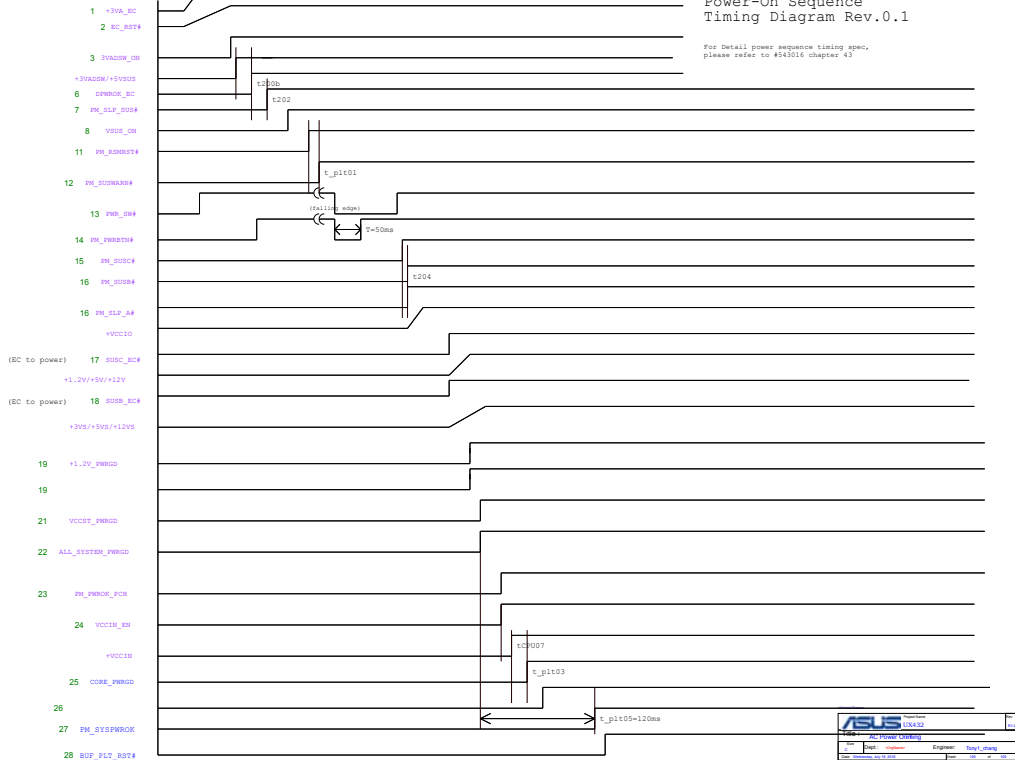
續續2008臺灣eACC臺灣有22萬家庭

## +FBVDDQ [For VRAM]







Power-On Sequence  
Timing Diagram Rev.0.1For Detail power sequence timing spec,  
please refer to #543016 chapter 43

Power On Sequence Diagram Rev.2.0

